Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): An arithmetic unit comprising:

a memory for storing data;

an arithmetic logic unit for executing a predetermined arithmetic operation with respect to [[a]] the data from the memory to provide first output data, the data being grouped into one of several patterns;

a register for temporarily storing the data read from the memory, and providing the temporarily stored data as second output data; and

a combining circuit for receiving [[a]] the first output data from the arithmetic logic unit and [[a]] the second output data from the register, and outputting combined data which is provided by replacing a part of the [[first]] second output data with [[and]] a part of the ~~second~~ first output data based on the pattern of the data from the memory,

wherein when the part of the second output data is replaced with the part of the first output data, the combining circuit shifts a position of data to be replaced in the second output data by a predetermined number of bits every time an operation process is executed.

Claim 2 (Canceled)

Claim 3 (Original): An arithmetic unit according to claim 1, wherein the memory includes a plurality of memory blocks.

Claim 4 (Canceled)

Claim 5 (Original): An arithmetic unit according to claim 1, further comprising a shifter for shifting data received from the memory and outputting the shifted data to the arithmetic logic unit.

Claim 6 (Original): An arithmetic unit according to claim 1, further comprising an accumulator for temporary storing data output from the arithmetic logic unit.

Claims 7-20 (Canceled)

Claim 21 (New): An arithmetic unit comprising:

a memory storing data;

an arithmetic logic unit executing a predetermined arithmetic operation with respect to the data from the memory to provide first output data, the data being grouped into one of several patterns;

a register temporarily storing the data read from the memory, and providing the temporarily stored data as second output data; and

a combining circuit that carries out an operation process by receiving the first output data from the arithmetic logic unit and the second output data from the register, replacing a part of the second output data from the register with a part of the first output data from the arithmetic logic unit based on the pattern of the data from the memory to provide combined data, and outputting the combined data to the memory for storage.

Claim 22 (New): An arithmetic unit according to claim 21, wherein the combining circuit shifts a position of data to be replaced in the second output data by a predetermined number of bits each successive operation process.

Claim 23 (New): An arithmetic unit according to claim 21, wherein the memory includes a plurality of memory blocks.

Claim 24 (New): An arithmetic unit according to claim 21, further comprising a shifter for shifting data received from the memory and outputting the shifted data to the arithmetic logic unit.

Claim 25 (New): An arithmetic unit according to claim 21, further comprising an accumulator for temporary storing data output from the arithmetic logic unit.